AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): A memory system comprising:

a plurality of memory modules provided with memory areas for holding data and buffer sections for sending and receiving the data;

a hard disk device to which the data stored in said memory modules is copied;

a control device for, in replacing an arbitrary memory module, switching a ring bus from a unidirectional bus capable of sending and receiving a signal unidirectionally to a bi-directional bus capable of either sending ~~and~~ or receiving a signal bi-directionally, detecting an address space of said memory module to be replaced, and accessing a memory area in said hard disk device corresponding to the detected address space at the time when an access to said memory module to be replaced is requested; and

a CPU which controls said control device for access operation to said memory modules,

wherein said buffer sections are connected in series to form the ring bus with said control device, each having a buffer circuit for causing said ring bus to operate as said unidirectional bus or said bi-directional bus in accordance with an instruction from said control device.

2. (currently amended): A memory system comprising:

a plurality of memory modules provided with memory areas for holding data and buffer sections for sending and receiving the data;

a hard disk device to which the data stored in said memory modules is copied;

a storage to which data stored in an arbitrary memory module is temporarily copied;

a control device for, in replacing an arbitrary memory module, switching a ring bus from a unidirectional bus capable of either sending ~~and~~ or receiving a signal unidirectionally to a bi-directional bus capable of sending and receiving a signal bi-directionally, detecting an address space of said memory module to be replaced, copying data corresponding to the detected address space from said hard disk device to said storage, and accessing a memory area in said storage corresponding to the detected address space at the time when an access to said memory module to be replaced is requested; and

a CPU which controls said control device for access operation to said memory modules,

wherein said buffer sections are connected in series to form the ring bus with said control device, each having a buffer circuit for causing said ring bus to operate as said unidirectional bus or said bi-directional bus in accordance with an instruction from said control device.

3. (original): The memory system according to claim 1, further comprising a short-circuit device for, when an arbitrary memory module is replaced, recovering bus connection which is disconnected by removing said memory module.

4. (original): The memory system according to claim 2, further comprising a short-circuit device for, when an arbitrary memory module is replaced, recovering bus connection which is disconnected by removing said memory module.

5. (currently amended): A memory system comprising:

a plurality of memory modules provided with memory areas for holding data and buffer sections for sending and receiving the data;

a hard disk device to which the data stored in said memory modules is copied;

a storage to which data stored in an arbitrary memory module is temporarily copied;

a short-circuit device for, in replacing an arbitrary memory module, recovering bus connection which is disconnected by removing said memory module to be replaced;

a control device for, in replacing an arbitrary memory module, detecting an address space of said memory module to be replaced, copying data corresponding to the detected address space from said hard disk device to said storage, and accessing a memory area in said storage corresponding to the detected address space at the time when an access to said memory module to be replaced is requested; and

a CPU which controls said control device for access operation to said memory modules,

wherein said buffer sections are connected in series to form a unidirectional bus capable of either sending ~~and~~ or receiving a signal unidirectionally.

6. (original): The memory system according to claim 3, wherein said short-circuit device is a dummy module which is inserted instead of said memory module to be replaced and is provided with a short-circuit line for short-circuiting bus connection which is disconnected by removing said memory module.

7. (original): The memory system according to claim 4, wherein said short-circuit device is a dummy module which is inserted instead of said memory module to be replaced and

is provided with a short-circuit line for short-circuiting bus connection which is disconnected by removing said memory module.

8. (original): The memory system according to claim 5, wherein said short-circuit device is a dummy module which is inserted instead of said memory module to be replaced and is provided with a short-circuit line for short-circuiting bus connection which is disconnected by removing said memory module.

9. (original): The memory system according to claim 3, wherein said short-circuit device is an FET switch, which is provided in association with said memory modules, respectively, for short-circuiting or opening bus connection which is disconnected by removing said memory module, and

in replacing an arbitrary memory module, said control device generates a control signal for turning ON the FET switch provided in association with said memory module to be replaced and turning OFF the FET switches provided in association with the other memory modules.

10. (original): The memory system according to claim 4, wherein said short-circuit device is an FET switch, which is provided in association with said memory modules, respectively, for short-circuiting or opening bus connection which is disconnected by removing said memory module, and

in replacing an arbitrary memory module, said control device generates a control signal for turning ON the FET switch provided in association with said memory module to be replaced and turning OFF the FET switches provided in association with the other memory modules.

11. (original): The memory system according to claim 5, wherein said short-circuit device is an FET switch, which is provided in association with said memory modules, respectively, for short-circuiting or opening bus connection which is disconnected by removing said memory module, and

in replacing an arbitrary memory module, said control device generates a control signal for turning ON the FET switch provided in association with said memory module to be replaced and turning OFF the FET switches provided in association with the other memory modules.

12. (original): The memory system according to claim 3, wherein said short-circuit device is a connector, which is provided in association with said memory modules, respectively, and is provided with short pins which short-circuits bus connection, which is disconnected by removing said memory module, at the time when said memory module is removed, and releases the short-circuit at the time when said memory module is inserted.

13. (original): The memory system according to claim 4, wherein said short-circuit device is a connector, which is provided in association with said memory modules, respectively, and is provided with short pins which short-circuits bus connection, which is disconnected by removing said memory module, at the time when said memory module is removed, and releases the short-circuit at the time when said memory module is inserted.

14. (original): The memory system according to claim 5, wherein said short-circuit device is a connector, which is provided in association with said memory modules, respectively, and is provided with short pins which short-circuits bus connection, which is disconnected by

removing said memory module, at the time when said memory module is removed, and releases the short-circuit at the time when said memory module is inserted.

15. (previously presented): The memory system according to claim 2, wherein said storage is a memory module for mirroring which is provided with a memory area for holding data and a buffer section for sending and receiving data.

16. (previously presented): The memory system according to claim 5, wherein said storage is a memory module for mirroring which is provided with a memory area for holding data and a buffer section for sending and receiving data.

17. (original): The memory system according to claim 2, wherein said storage is a memory for graphics.

18. (original): The memory system according to claim 5, wherein said storage is a memory for graphics.

19. (original): The memory system according to claim 2, wherein said storage is free memory areas of the other memory modules excluding said memory module to be replaced.

20. (original): The memory system according to claim 5, wherein said storage is free memory areas of the other memory modules excluding said memory module to be replaced.

21. (currently amended): A control method for a memory system which has a plurality of memory modules provided with memory areas for holding data and buffer sections for sending and receiving the data,

wherein said buffer sections are connected in series to form a ring bus with a control device which controls an operation for accessing memory modules, said method comprising the steps of:

copying the data stored in said memory modules to a hard disk device at each predetermined period;

in replacing an arbitrary memory module, switching said ring bus from a unidirectional bus capable of either sending ~~and~~ or receiving a signal unidirectionally to a bi-directional bus capable of sending and receiving a signal bi-directionally;

detecting an address space of said memory module to be replaced; and

accessing a memory area in said hard disk device corresponding to the detected address space at the time when an access to said memory module to be replaced is requested.

22. (currently amended): A control method for a memory system which has a plurality of memory modules provided with memory areas for holding data and buffer sections for sending and receiving the data,

wherein said buffer sections are connected in series to form a ring bus with a control device which controls an operation for accessing memory modules, said method comprising the steps of:

copying the data stored in said memory modules to a hard disk device at each predetermined period;

in replacing an arbitrary memory module, switching said ring bus from a unidirectional bus capable of either sending ~~and~~ or receiving a signal unidirectionally to a bi-directional bus capable of sending and receiving a signal bi-directionally;

detecting an address space of said memory module to be replaced;

copying data corresponding to the detected address space from said hard disk device to a storage; and

accessing a memory area in said storage corresponding to the detected address space at the time when an access to said memory module to be replaced is requested.

23. (currently amended): A control method for a memory system which has a plurality of memory modules provided with memory areas for holding data and buffer sections for sending and receiving the data,

wherein said buffer sections are connected in series to form a unidirectional bus capable of either sending ~~and~~ or receiving a signal unidirectionally, said method comprising the steps of:

copying the data stored in said memory modules to a hard disk device at each predetermined period;

in replacing an arbitrary memory module, short-circuiting bus connection which is disconnected by removing said memory module to be replaced;

detecting an address space of said memory module to be replaced;

copying data corresponding to the detected address space from said hard disk device to a storage; and

accessing a memory area in said storage corresponding to the detected address space at the time when an access to said memory module to be replaced is requested.

24. (original): The control method for a memory system according to claim 21, further comprising the step of:

in replacing an arbitrary memory module, inserting a dummy module provided with a short-circuit line for short-circuiting a bus, which is disconnected by removing said memory module, instead of said memory module to be replaced.

25. (original): The control method for a memory system according to claim 22, further comprising the step of:

in replacing an arbitrary memory module, inserting a dummy module provided with a short-circuit line for short-circuiting a bus, which is disconnected by removing said memory module, instead of said memory module to be replaced.

26. (original): The control method for a memory system according to claim 23, further comprising the step of:

in replacing an arbitrary memory module, inserting a dummy module provided with a short-circuit line for short-circuiting a bus, which is disconnected by removing said memory module, instead of said memory module to be replaced.

27. (original): The control method for a memory system according to claim 21, further comprising the step of:

in replacing an arbitrary memory module, turning ON an FET switch, which is provided in association with said memory module to be replaced, for short-circuiting or opening a bus which is disconnected by removing said memory module, and turning OFF said FET switch provided in association with the other memory modules.

28. (original): The control method for a memory system according to claim 22, further comprising the step of:

in replacing an arbitrary memory module, turning ON an FET switch, which is provided in association with said memory module to be replaced, for short-circuiting or opening a bus which is disconnected by removing said memory module, and turning OFF said FET switch provided in association with the other memory modules.

29. (original): The control method for a memory system according to claim 23, further comprising the step of:

in replacing an arbitrary memory module, turning ON an FET switch, which is provided in association with said memory module to be replaced, for short-circuiting or opening a bus which is disconnected by removing said memory module, and turning OFF said FET switch provided in association with the other memory modules.

30. (original): The control method for a memory system according to claim 21, further comprising the step of:

in replacing an arbitrary memory module, short-circuiting short pins, which are provided in a connector corresponding to said memory module to be replaced, for short-circuiting or opening a bus which is disconnected by removing said memory module to be replaced, and releasing the short-circuit of said short pins provided in association with the other memory modules.

31. (original): The control method for a memory system according to claim 22, further comprising the step of:

in replacing an arbitrary memory module, short-circuiting short pins, which are provided in a connector corresponding to said memory module to be replaced, for short-circuiting or opening a bus which is disconnected by removing said memory module to be replaced, and releasing the short-circuit of said short pins provided in association with the other memory modules.

32. (original): The control method for a memory system according to claim 23, further comprising the step of:

in replacing an arbitrary memory module, short-circuiting short pins, which are provided in a connector corresponding to said memory module to be replaced, for short-circuiting or opening a bus which is disconnected by removing said memory module to be replaced, and releasing the short-circuit of said short pins provided in association with the other memory modules.

33. (previously presented): The control method for a memory system according to claim 22, wherein said storage is a memory for mirroring provided with a memory area for holding data and a buffer section for sending and receiving data.

34. (previously presented): The control method for a memory system according to claim 23, wherein said storage is a memory for mirroring provided with a memory area for holding data and a buffer section for sending and receiving data.

35. (original): The control method for a memory system according to claim 22, wherein said storage is a memory for graphics.

36. (original): The control method for a memory system according to claim 23, wherein said storage is a memory for graphics.

37. (original): The control method for a memory system according to claim 22, wherein said storage is free memory areas of the other memory modules excluding said memory module to be replaced.

38. (original): The control method for a memory system according to claim 23, wherein said storage is free memory areas of the other memory modules excluding said memory module to be replaced.